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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,861	08/20/2003	Wingyu Leung	MST-012-1P	7697

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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,861	LEUNG ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 705,1004,404,304.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1: "correcting a single-bit error in the test data pattern and the corresponding ECC value if a single-bit error exists in the test data pattern and the corresponding ECC value" is apparently unclear and confusing and apparently should be "correcting a single-bit error in the combination of test data pattern and ~~the~~ corresponding ECC value if a single-bit error exists in the combination of test data pattern and ~~the~~ corresponding ECC value," and "ensuring that an erroneous test data pattern having one or more error bits is provided if the test data pattern and the corresponding ECC value include a multiple bit error" is apparently unclear and confusing and apparently should be "ensuring that an erroneous test data pattern having one or more error bits is provided if the combination of test data pattern and ~~the~~ corresponding ECC value include a multiple bit error."

Regarding claims 2 and 7: "the test data pattern and the corresponding ECC value" apparently should be "the combination of test data pattern and ~~the~~ corresponding ECC value."

Regarding claim 6: "the test data pattern and the ECC value" apparently should be "the combination of test data pattern and ~~the~~ ECC value."

Regarding claim 9: "patterns having one or more error bits are provided if multiple-bit errors exist in the retrieved test data patterns and the corresponding ECC values" is vague and apparently should be "~~patterns~~ a pattern having one or more error bits ~~are~~ is provided if a multiple-bit ~~errors exist~~ error exists in ~~the~~ a combination of retrieved test data ~~patterns~~ pattern and ~~the~~ corresponding ECC ~~values~~ value."

Regarding claims 11 (one occurrence) and 12 (two occurrences): "each of the retrieved test data patterns and corresponding ECC values" apparently should be "~~each~~ any combination of ~~the~~ retrieved test data ~~patterns~~ pattern and corresponding ECC ~~values~~ value."

Regarding claim 19: "correct single bit errors the test data patterns and the corresponding ECC values" apparently should be "correct a single bit ~~errors~~ error in any combination of ~~the~~ test data ~~patterns~~ pattern and ~~the~~ corresponding ECC ~~values~~ value," and "multiple-bit error in a test data pattern and the corresponding ECC value" apparently should be "multiple-bit error in a combination of test data pattern and ~~the~~ corresponding ECC value."

Regarding claim 20: "correct single bit errors in the test data pattern and the corresponding ECC value" apparently should be "correct a single bit ~~errors~~ error in any combination of ~~the~~ test data pattern and ~~the~~ corresponding ECC value," and "a multiple-bit error exists in the test data pattern and the corresponding ECC value" apparently

should be "a multiple-bit error exists in a combination of ~~the~~ test data pattern and ~~the~~ corresponding ECC value."

Regarding claim 22: "the test data pattern and the corresponding ECC value" apparently should be "the combination of test data pattern and ~~the~~ corresponding ECC value."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-17 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,274,646 to Brey et al (hereafter "Brey").

Brey discloses a semiconductor memory system with ECC coding wherein each (72, 64) ECC codeword (*i.e.* a combination of "data pattern" and "ECC value") of an odd-weight Hamming code is capable of correcting a single bit error and detecting a double error. Decoding includes generating a syndrome by comparing the stored ECC redundancy to regenerated ECC redundancy. In the case of a single error, the "data pattern" is corrected before being passed to the requestor. In the case of a double error, the "data pattern" is passed with the error intact (col. 6, lines 48-52) thereby "ensuring that an erroneous ... data pattern having ... error bits is provided if the ... data pattern

and the corresponding ECC ... include a multiple-bit error, and passing the erroneous ... data pattern as an output."

Brey does not describe the data to be written and read to the semiconductor memory as "test data." Official Notice is given that the usefulness in applying test data patterns to a semiconductor memory in a semiconductor memory system in order to ensure correct operation of the semiconductor memory system was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read test data from the semiconductor memory in the semiconductor memory system disclosed by Brey. Such an application would have been obvious because the usefulness in applying test data patterns to a semiconductor memory in a semiconductor memory system in order to ensure correct operation of the semiconductor memory system was already well known.

Regarding claims 2, 15-17 and 23, Official Notice is given that marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to write to and read marching "0" and marching "1" test data from the semiconductor memory in the semiconductor memory system disclosed by Brey. Such an application would have been obvious because marching "0" and marching "1" patterns were well known test patterns for testing semiconductor memories.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb